a) defining a phantom port containing a plurality of sequential memory addresses;

b) generating an address to the phantom port using a conventional addressing scheme;

c) determining an address in memory address space corresponding to the generated phantom port address; and

d) accessing the address in memory address space.

22. (Amended) A system for remapping between pixel coordinate space and memory address space, comprising:

a central processing unit;

a frame buffer memory coupled to the central processing unit and having an associated memory address scheme;

a memory address device coupled to the central processing unit for defining a phantom port containing a plurality of sequential memory addresses, each of a subset of the memory addresses mapping to an address in the frame buffer memory; and

a remapping device coupled to the memory address device for converting an address between the memory address scheme of the frame buffer memory and a memory address of the phantom port.

REMARKS

Claims 1-29 are pending after this amendment. Claims 1 and 22 have been amended.

The Examiner rejected claims 1-17 and 19-29 under 35 U.S.C. §103(a) as being unpatentable over Applicant's Fig. 1 in view of Nagashima or Wilde or Wang et al. This rejection is respectfully traversed.